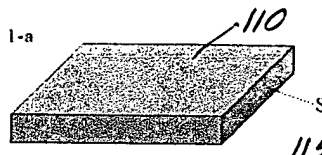
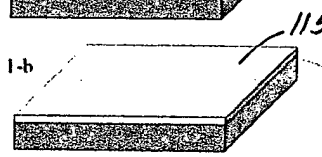
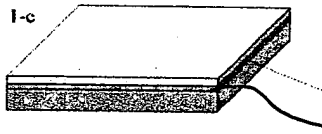


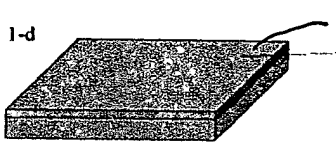
Starting material: Intrinsic Si <100>, double side polished.



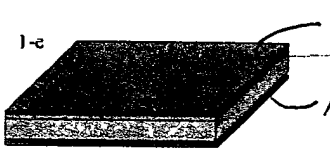
Spin on dopant (SOD) consisting of borosilicate glass. Bake at 170 °C for 1 minute.



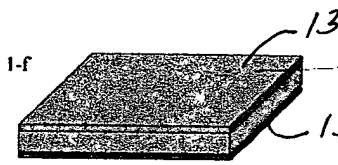
Annealing at 1100 °C, remove when desired implant thickness has been reached



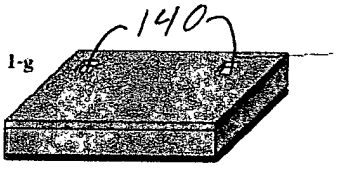
Strip SOD with dilute HF



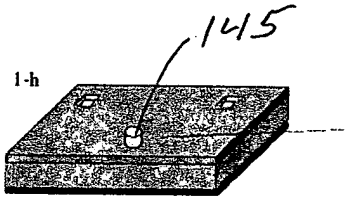
Deposit 200 nm of Si_3N_4



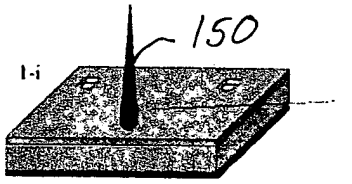
Strip Si_3N_4 from front



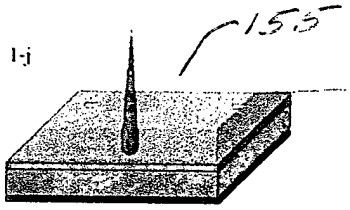
Define alignment marks on top side of wafer using photolithography and RIE



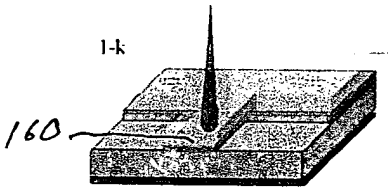
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff



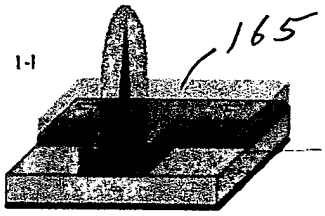
Grow high aspect ratio VACNF using catalytic PECVD



Deposit conformal layer of PECVD SiO_2 onto the top side of the wafer to protect the VACNF



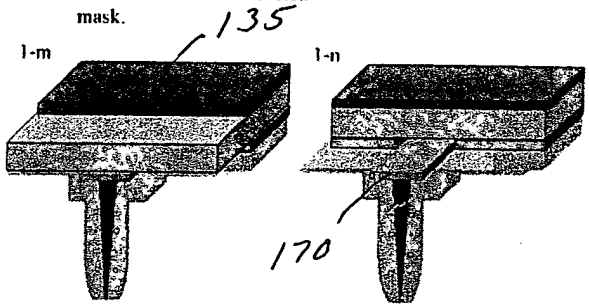
Pattern the cantilever body using photolithography and RIE

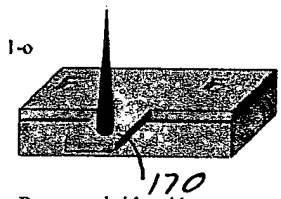


Deposit 200 nm of Si_xN_y on to wafer surface to protect during KOH etching

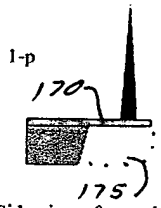
Pattern nitride on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.

Pattern the Si using heated KOH.

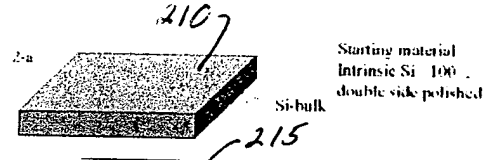




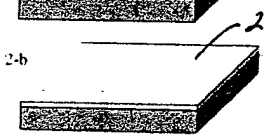
Remove nitride with RIE and oxide using a wet etch in HF.



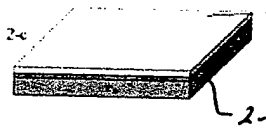
Side view of completed cantilever structure



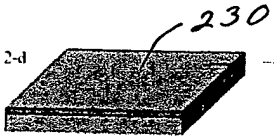
Starting material Intrinsic Si 100 , double side polished



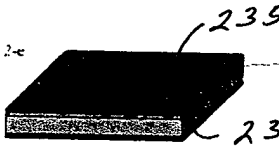
Borosilicate glass, spin on dopant, bake at 170 °C for 1 minute.



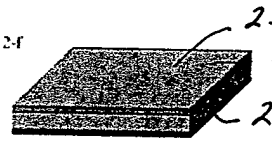
Put in annealing furnace at 1100 °C, remove when desired implant thickness has been reached.



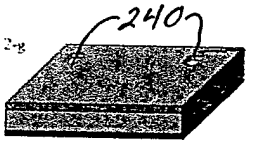
Strip SOD with dilute HF



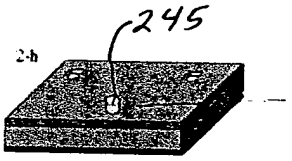
Deposit 200 nm of Si_3N_4



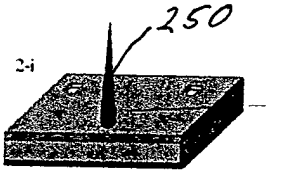
Strip Si_3N_4 from front



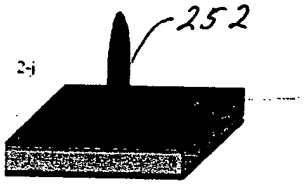
Define alignment marks on top side of wafer using photolithography and RIE



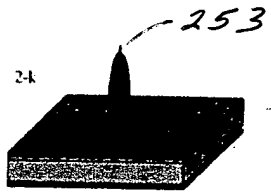
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff



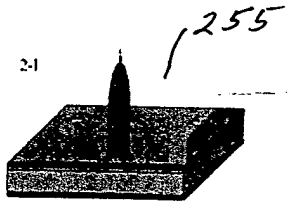
Grow high aspect ratio VACNF using catalytic PECVD



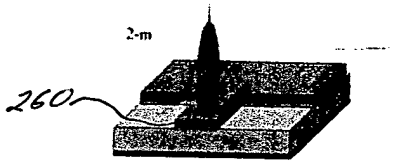
Deposit thin layer of Si_3N_4



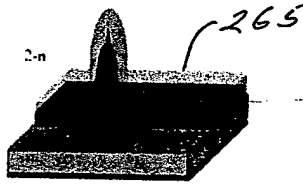
Remove Si_3N_4 from tip using photoresist and RIE



Deposit conformal layer of PECVD SiO_2 onto the top side of the wafer to protect the VACNT



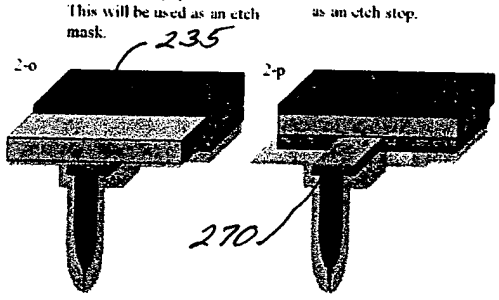
Pattern the cantilever body using photolithography and RIE

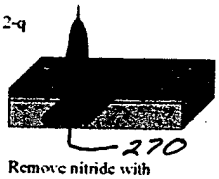


Deposit 200 nm of Si_3N_4 on to wafer surface to protect during KOH etching

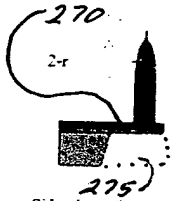
Pattern nitride on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.

Pattern the Si using KOH. The nitride on the front side functions as an etch stop.

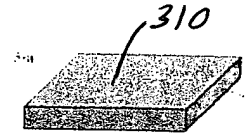




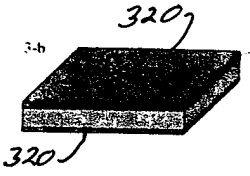
Remove nitride with RIE and oxide using a wet etch in HF.



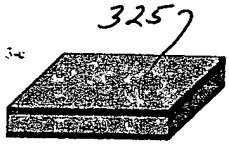
Side view of completed cantilever structure



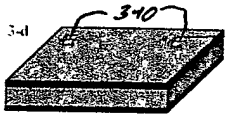
Starting material: Intrinsic Si <100> double side polished.



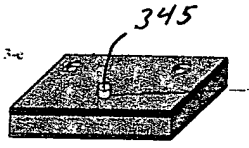
Deposit LPCVD low stress Si_3N_4 and strip from back using RIE if necessary



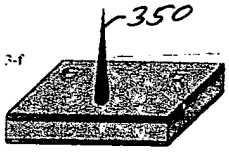
PVD W



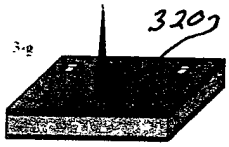
Define alignment marks on top side of wafer using photolithography and RIE



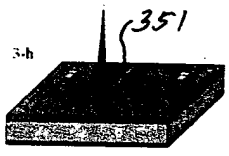
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff



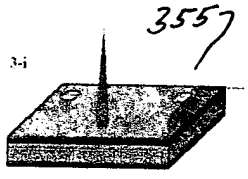
Grow high aspect ratio VACNF using catalytic PECVD



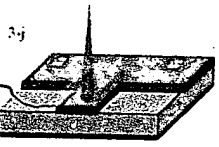
Remove W layer using RIE



Alternatively, the W layer can be patterned using photolithography and RIE to provide an electrical interconnect to the VACNF base

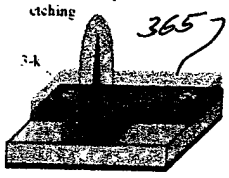


Deposit conformal layer of PECVD SiO2 onto the top side of the wafer to protect the VACNF

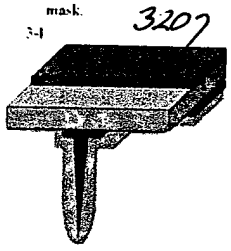


Pattern the cantilever body using photolithography and RIE

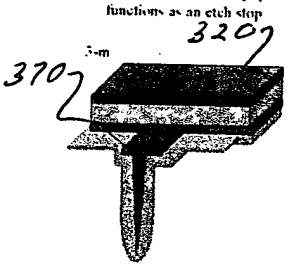
Deposit 200 nm of Si_3N_4 on to wafer surface to protect during KOH etching



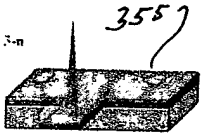
Pattern nitride on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.

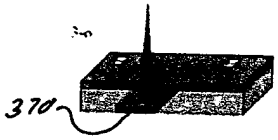


Pattern the Si using heated KOH. The Si_3N_4 functions as an etch stop

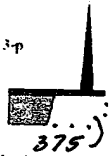


Remove Si_3N_4 membrane with RIE from front side

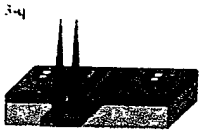


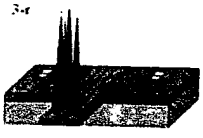


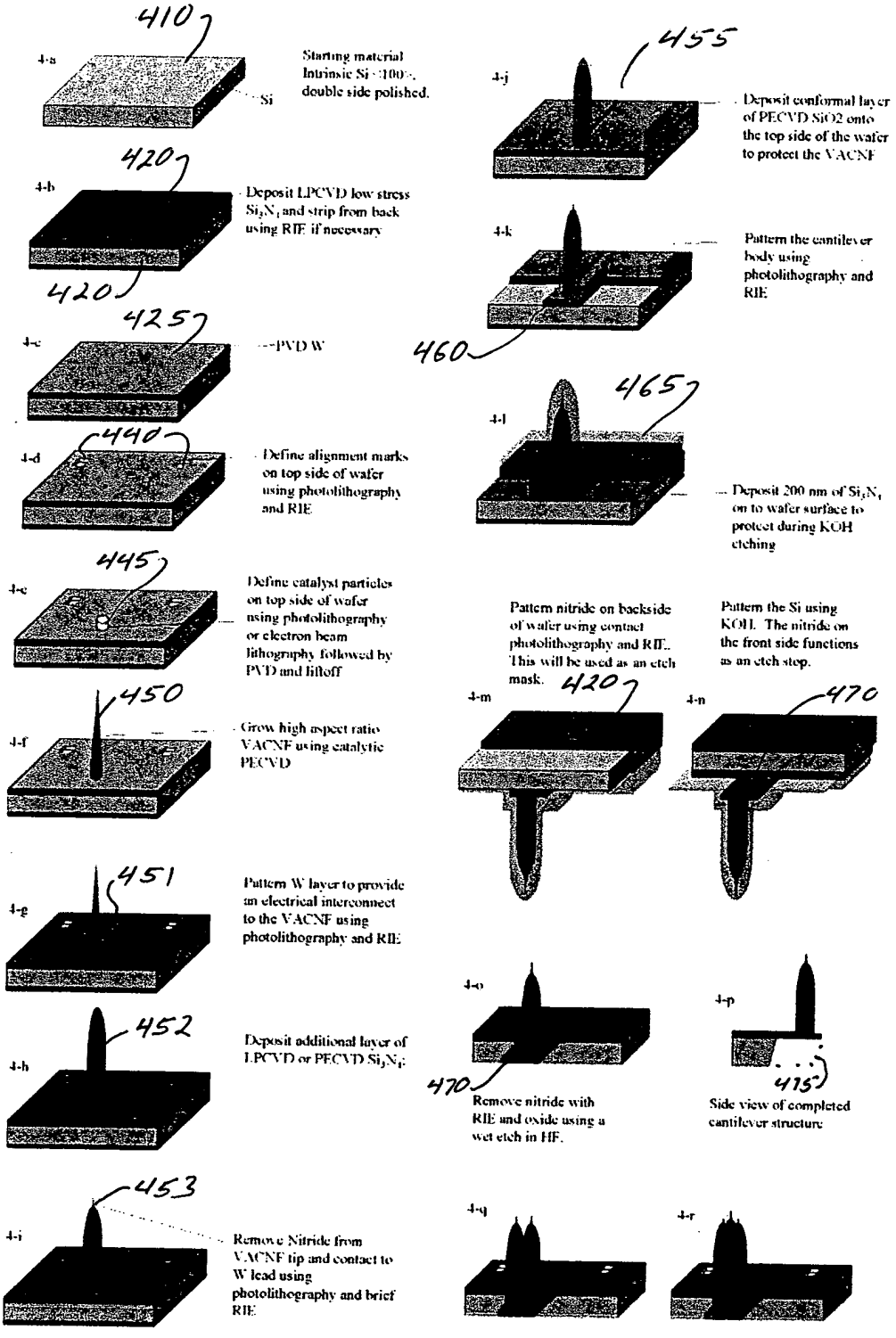
Remove oxide using a wet etch in HF completing the structure

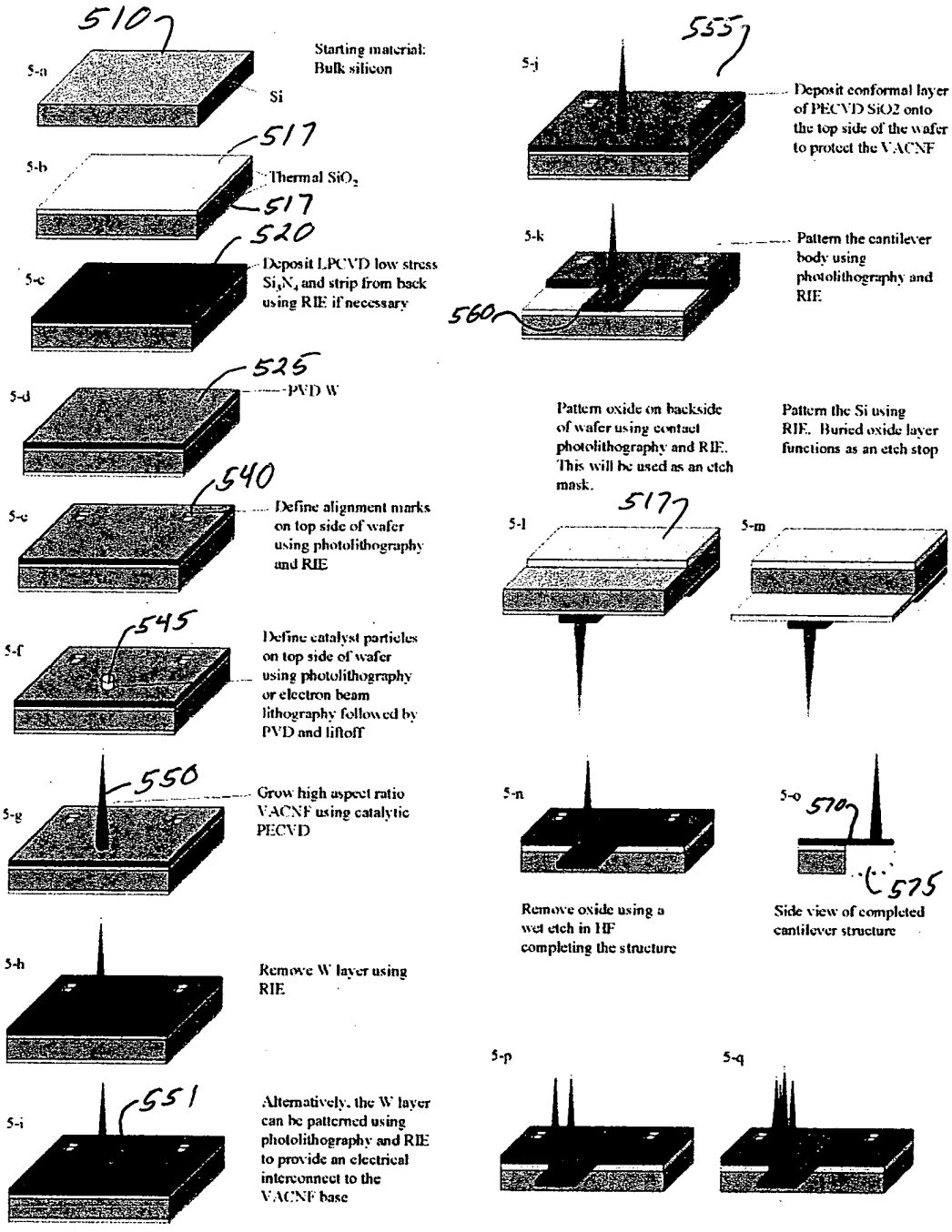


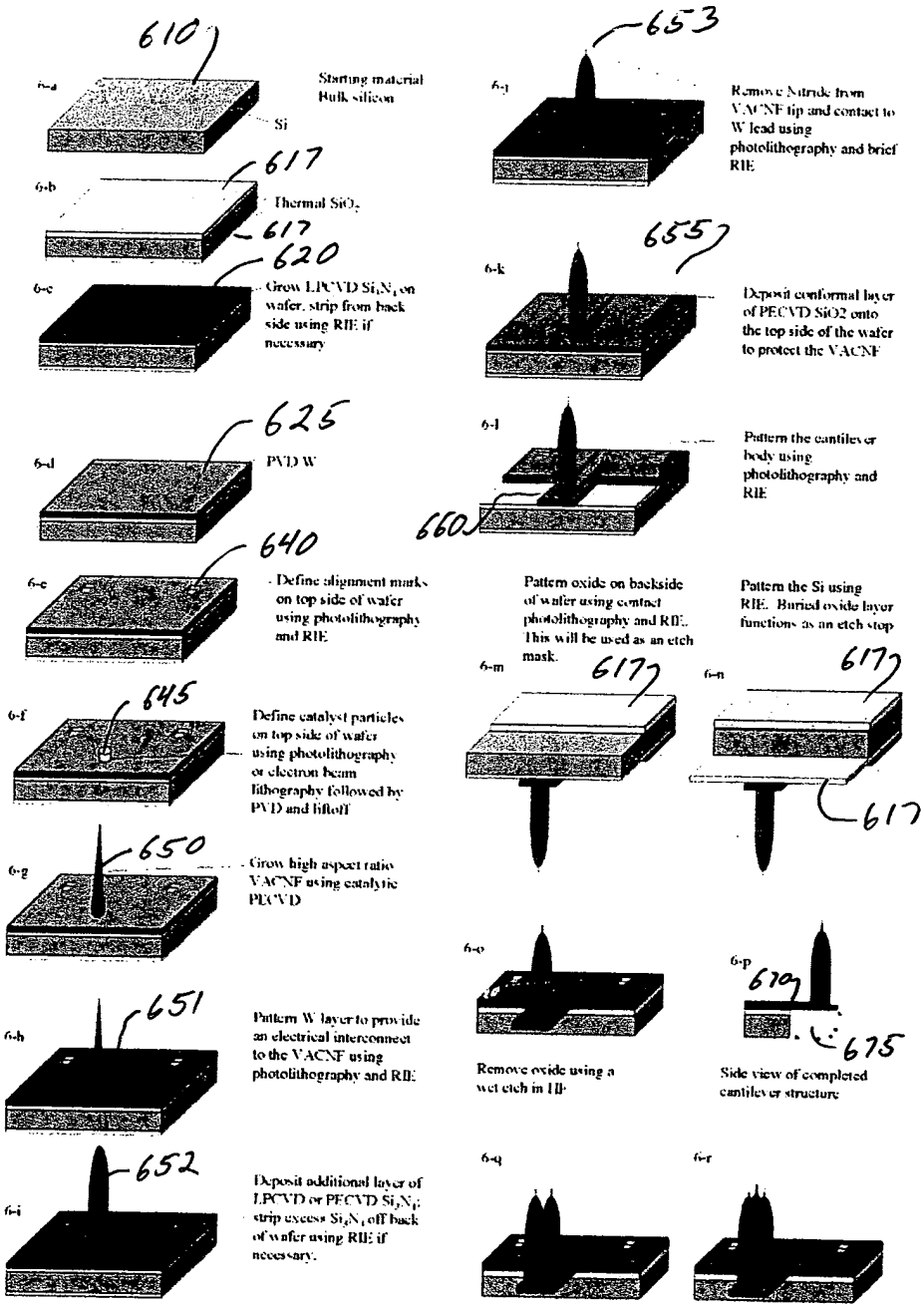
Side view of completed cantilever structure

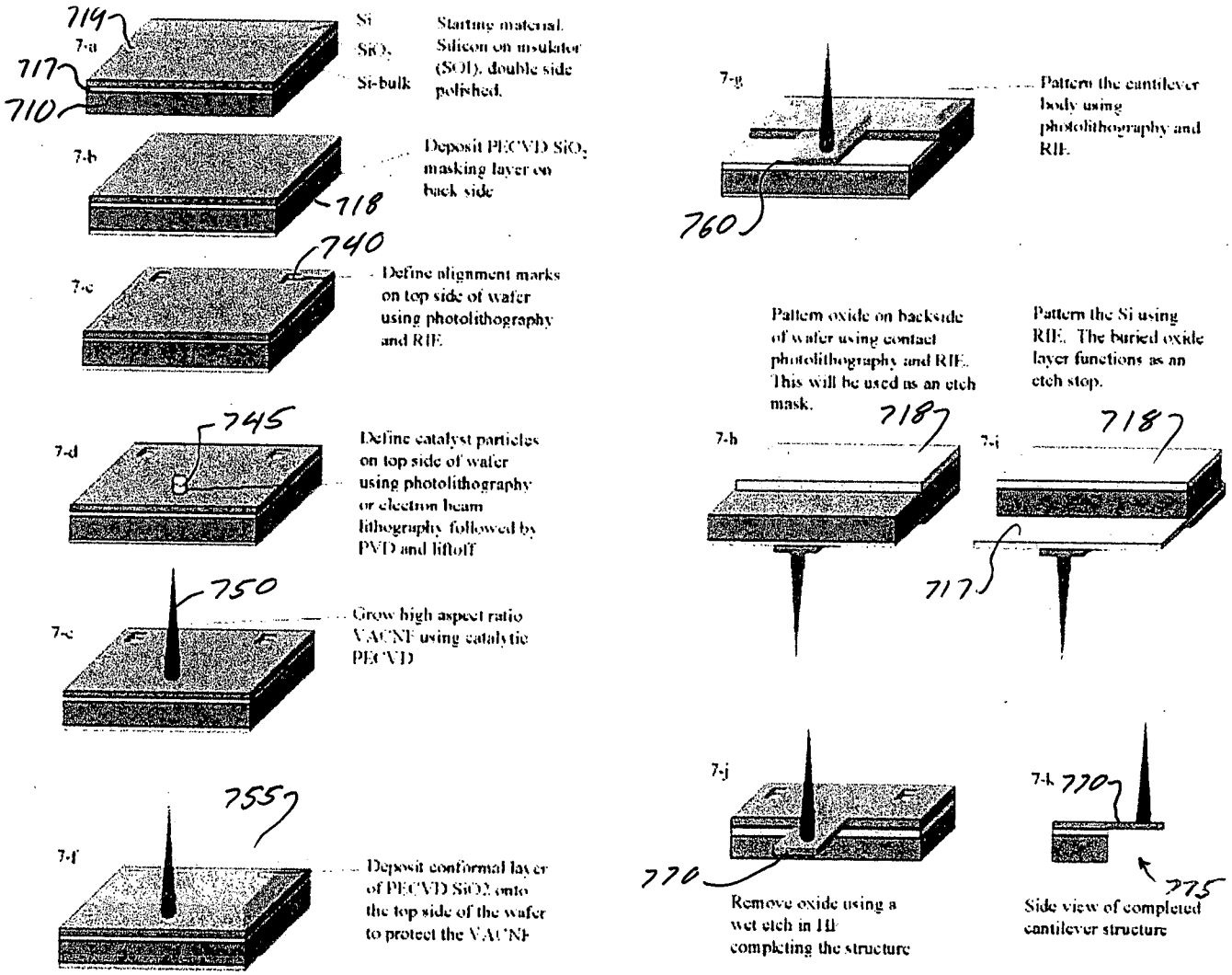


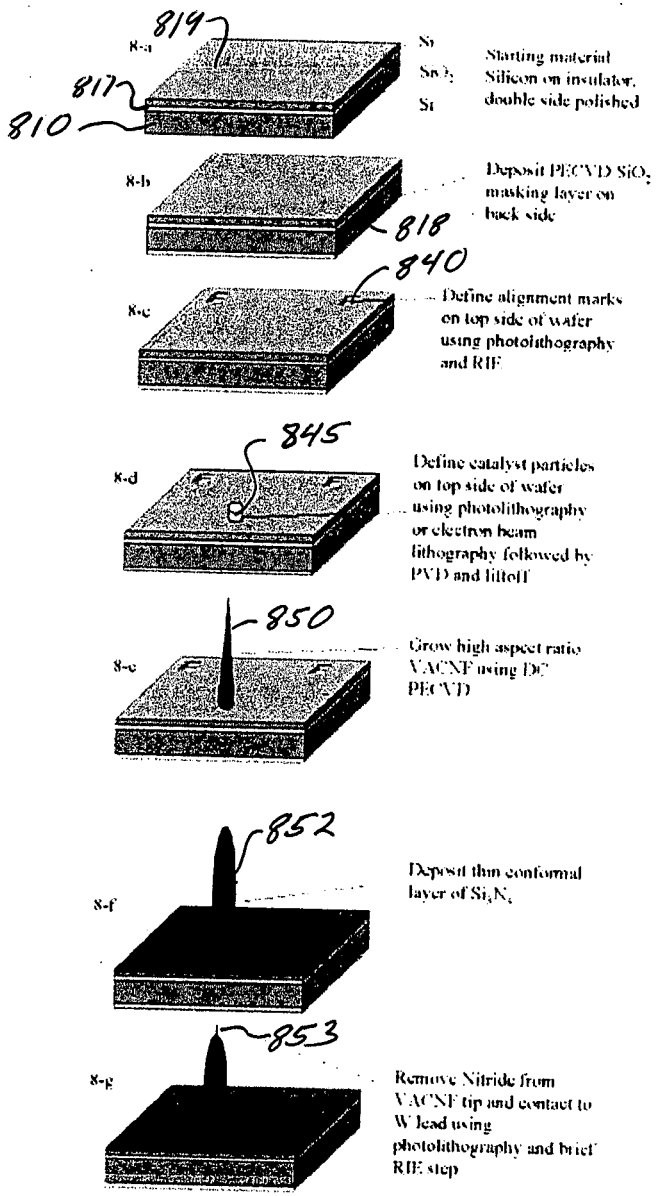


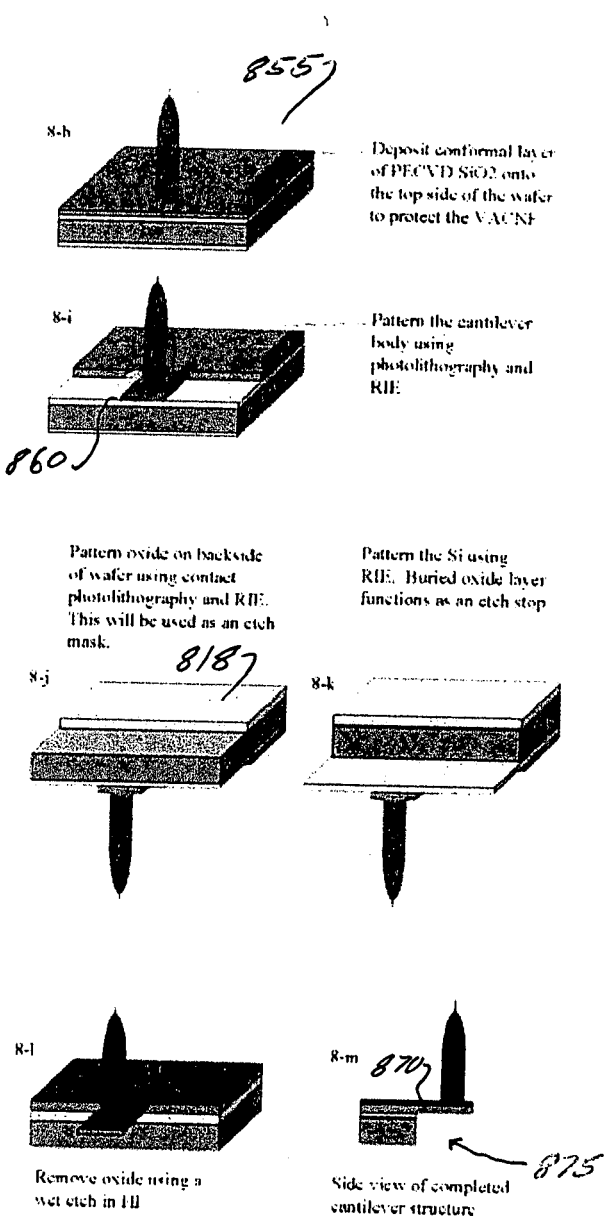

410
4-a
Si
Starting material Intrinsic Si <100>, double side polished.
420
4-b
Deposit LPCVD low stress Si_3N_4 and strip from back using RIE if necessary
420
425
4-c
PVD W
440
4-d
Define alignment marks on top side of wafer using photolithography and RIE
445
4-e
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff
450
4-f
Grow high aspect ratio VACNF using catalytic PECVD
451
4-g
Pattern W layer to provide an electrical interconnect to the VACNF using photolithography and RIE
452
4-h
Deposit additional layer of LPCVD or PECVD Si_3N_4
453
4-i
Remove Nitride from VACNF tip and contact to W lead using photolithography and brief RIE
455
4-j
Deposit conformal layer of PECVD SiO2 onto the top side of the wafer to protect the VACNF
4-k
Pattern the cantilever body using photolithography and RIE
460
465
4-l
Deposit 200 nm of Si_3N_4 on to wafer surface to protect during KOH etching
Pattern nitride on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.
Pattern the Si using KOH. The nitride on the front side functions as an etch stop.
4-m
420
4-n
470
4-o
470
Remove nitride with RIE and oxide using a wet etch in HF.
4-p
475
Side view of completed cantilever structure
4-q
4-r


510
5-a
Starting material: Bulk silicon
Si
517
5-b
Thermal SiO_2
517
520
5-c
Deposit LPCVD low stress Si_3N_4 and strip from back using RIE if necessary
525
5-d
PVD W
540
5-e
Define alignment marks on top side of wafer using photolithography and RIE
545
5-f
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff
550
5-g
Grow high aspect ratio VACNF using catalytic PECVD
5-h
Remove W layer using RIE
551
5-i
Alternatively, the W layer can be patterned using photolithography and RIE to provide an electrical interconnect to the VACNF base
555
5-j
Deposit conformal layer of PECVD SiO2 onto the top side of the wafer to protect the VACNF
5-k
560
Pattern the cantilever body using photolithography and RIE
Pattern oxide on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.
Pattern the Si using RIE. Buried oxide layer functions as an etch stop
517
5-l
5-m
5-n
Remove oxide using a wet etch in HF completing the structure
5-o
570
575
Side view of completed cantilever structure
5-p
5-q


610
6-a
Starting material Bulk silicon
Si
617
6-b
Thermal SiO_2
617
620
6-c
Grow LPCVD Si_3N_4 on wafer, strip from back side using RIE if necessary
625
6-d
PVD W
640
6-e
Define alignment marks on top side of wafer using photolithography and RIE
645
6-f
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff
650
6-g
Grow high aspect ratio VACNF using catalytic PECVD
651
6-h
Pattern W layer to provide an electrical interconnect to the VACNF using photolithography and RIE
652
6-i
Deposit additional layer of LPCVD or PECVD Si_3N_4; strip excess Si_3N_4 off back of wafer using RIE if necessary.
653
6-j
Remove Nitride from VACNF tip and contact to W lead using photolithography and brief RIE
655
6-k
Deposit conformal layer of PECVD SiO2 onto the top side of the wafer to protect the VACNF
6-l
660
Pattern the cantilever body using photolithography and RIE
Pattern oxide on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.
Pattern the Si using RIE. Buried oxide layer functions as an etch stop
6-m
617
6-n
617
617
6-o
Remove oxide using a wet etch in HF
6-p
670
675
Side view of completed cantilever structure
6-q
6-r


714
7-a
717
710
Si
SiO2
Si-bulk
Starting material. Silicon on insulator (SOI), double side polished.
7-b
718
Deposit PECVD SiO2 masking layer on back side
740
7-c
Define alignment marks on top side of wafer using photolithography and RIE
745
7-d
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff
750
7-e
Grow high aspect ratio VACNF using catalytic PECVD
755
7-f
Deposit conformal layer of PECVD SiO2 onto the top side of the wafer to protect the VACNF
7-g
Pattern the cantilever body using photolithography and RIE
760
Pattern oxide on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.
Pattern the Si using RIE. The buried oxide layer functions as an etch stop.
718
7-h
7-i
717
7-j
770
Remove oxide using a wet etch in HF completing the structure
7-k
770
775
Side view of completed cantilever structure


814
817
810
8-a
Si
SiO_2
Si
Starting material
Silicon on insulator, double side polished
8-b
818
Deposit PECVD SiO_2 masking layer on back side
840
8-c
Define alignment marks on top side of wafer using photolithography and RIE
845
8-d
Define catalyst particles on top side of wafer using photolithography or electron beam lithography followed by PVD and liftoff
850
8-e
Grow high aspect ratio VACNF using DC PECVD
852
8-f
Deposit thin conformal layer of Si_3N_4
853
8-g
Remove Nitride from VACNF tip and contact to W lead using photolithography and brief RIE step


855
8-h
Deposit conformal layer of PECVD SiO2 onto the top side of the wafer to protect the VACNF
8-i
Pattern the cantilever body using photolithography and RIE
860
Pattern oxide on backside of wafer using contact photolithography and RIE. This will be used as an etch mask.
Pattern the Si using RIE. Buried oxide layer functions as an etch stop
818
8-j
8-k
8-l
Remove oxide using a wet etch in HF
8-m
870
875
Side view of completed cantilever structure

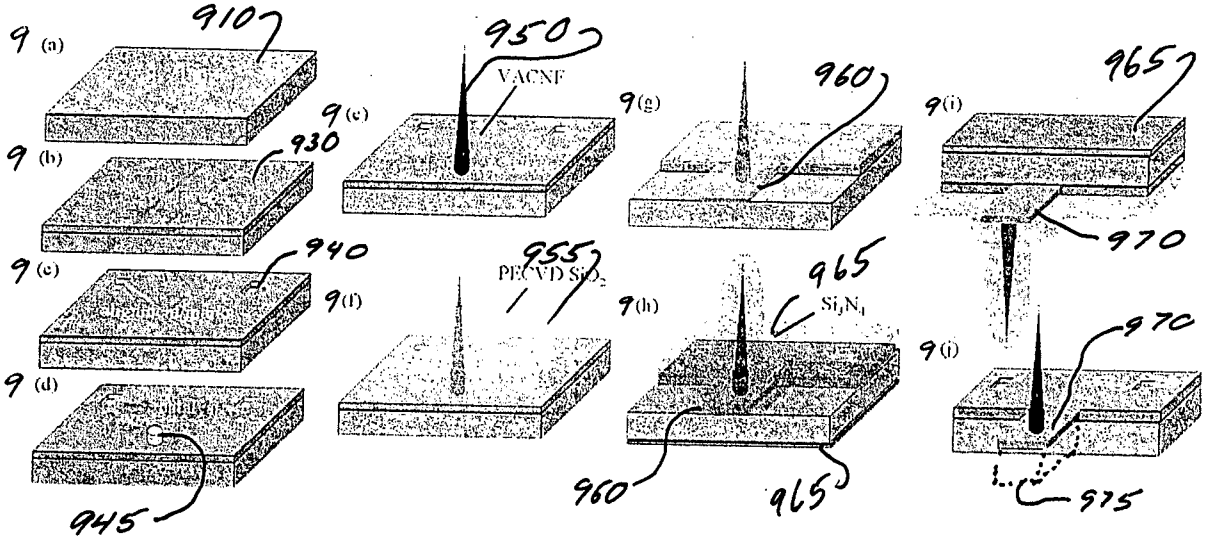
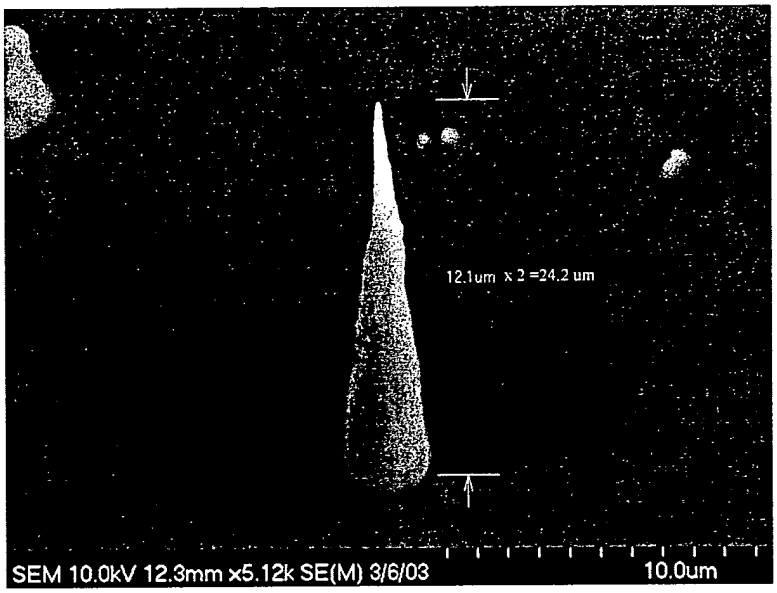

9 (a)
910
9 (b)
930
9 (c)
940
9 (d)
945
950
VACNF
9 (e)
9 (f)
955
PECVD SiO_2
9 (g)
960
9 (h)
965
Si_3N_4
960
965
9 (i)
965
970
9 (j)
970
975

Fig 10A



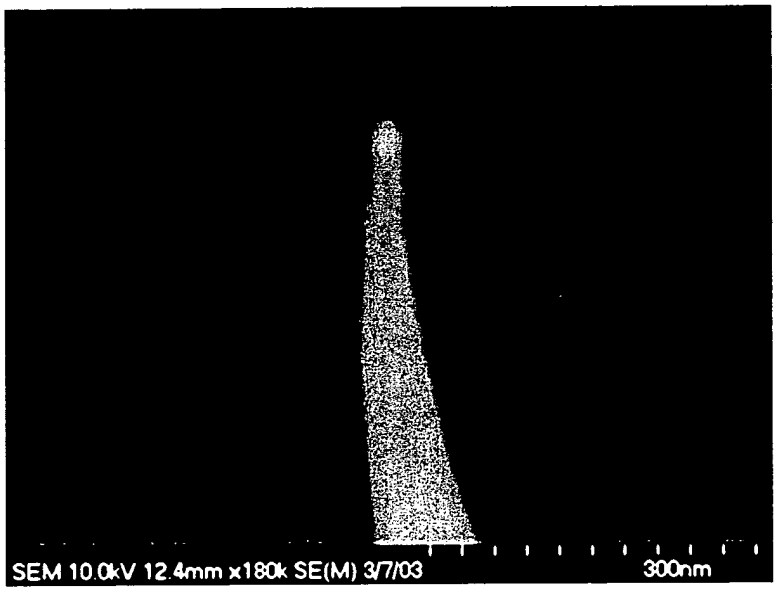


Fig 10B

Fig 11

Fig 12A

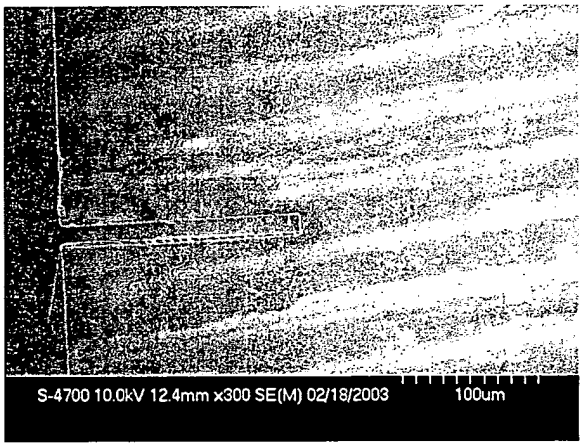
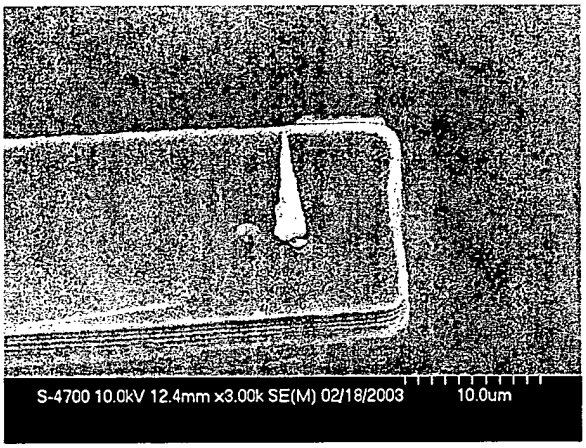


Fig 12B



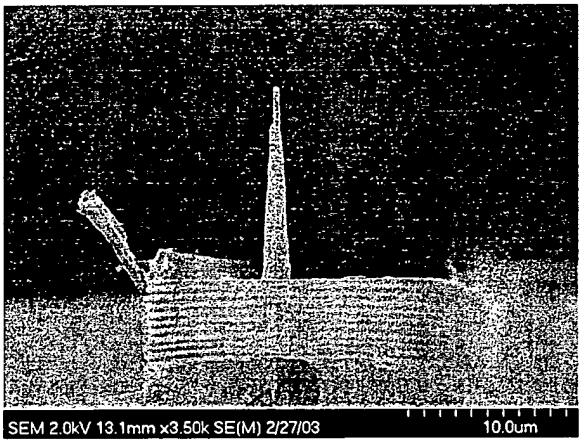


Fig 12C

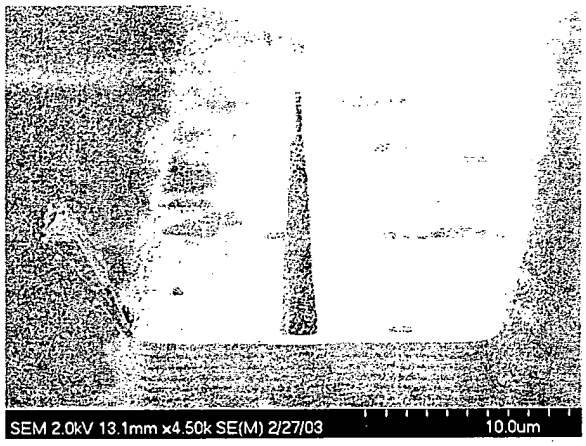


Fig 12D